EXHIBIT C

Mat. Res. Soc. Symp. Vol. 640 © 2001 Materials Research Society

Design and Process Issues for Silicon Carbide Power DiMOSFETS

Sei-Hyung Ryu[1], Anant K. Agarwal[1], Nelson S. Saks[2], Mrinal K. Das[1], Lori A. Lipkin[1], Ranbir Singh[1], and John W. Palmour[1]
[1]Cree, Inc., 4600 Silicon Drive
Durham, NC 27703
[2]Navel Research Laboratory, 4555 Overlook Avenue
Washington, D.C. 20375

ABSTRACT

This paper discusses the design and process issues of high voltage power DiMOSFETs (Double implanted MOSFETs) in 4H-silicon carbide (SiC). Since Critical Field (E_C) in 4H-SiC is very high (10X higher than that of a Si), special care is needed to protect the gate oxide. 2D device simulation tool was used to determine the optimal JFET gap, which provides adequate gate oxide protection as well as a reasonable JFET resistance. The other issue in 4H-SiC DiMOSFETs is extremely low effective channel mobility (μ_{eff}) in the implanted p-well regions. NO anneal of the gate oxide and buried channel structure are used for increasing μ_{eff}. NO anneal, which was reported to be very effective in increasing the μ_{eff} of SiC MOSFETS in p-type epilayers, did not produce reasonable μ_{eff} of SiC MOSFETs in the implanted p-well. Buried channel (BC) structure with 2.7×10^{12} cm^{-2} charge in the channel showed high μ_{eff} utilizing bulk buried channel, but resulted in a normally-on device. However, it was shown that by controlling the charge in the BC layer, a normally off device with high μ_{eff} can be produced. A 3.3 mm x 3.3 mm DiMOSFET with BC structure showed a drain current of 10 A, which is the highest current reported in SiC power MOSFETs to date, at a forward drop of 4.4 V with a gate bias of only 2.5 V.

INTRODUCTION

High voltage power DiMOSFETs (Double implanted MOSFETs) [1] in silicon carbide (SiC) are very attractive because they have potentials to match silicon IGBTs in the on-state drop, but offer superior switching speed. In SiC power DiMOSFETs, the peak electric field in the blocking region is designed to be approximately 10X higher than that of a Si device with equivalent blocking voltage. This can be detrimental to gate oxide if adequate shielding of electric field is not provided. In this paper, SiC DiMOSFETs with JFET gaps ranging from 2 μm to 5 μm is studied using a 2D device simulator to determine an optimal compromise between gate oxide protection and JFET resistance for 2000V 4H-SiC DiMOSFETs.

Another important issue for SiC DiMOSFETs is extremely low surface channel mobility, especially in 4H-SiC. Several methods, such as channel implantations[2] and different anneals for gate dielectric[3,4] have been suggested to improve the MOS channel mobility. These methods were successful for simple devices built in lightly doped p-type epilayers. However, high channel mobility in implanted p-wells, which is more practical for power MOSFETs, have yet to be demonstrated. In this paper, FATFET results in implanted p-wells are obtained for devices with NO anneal and with buried channel structure, and characteristics of power DiMOSFETs fabricated using these techniques are presented.

DEVICE DESIGN AND PROCESSING

Figure 1 shows a simple schematic cross-section of a DiMOSFET cell. MOS channel length is defined by two separate implants (p-well and n^+ implants). Electrons flow from n^+ source through a MOS channel on the implanted p-well, then through the JFET region formed by two adjacent p-well regions, and then through lightly doped n^- drift region into the drain. Blocking voltage of this device is determined by the doping and the thickness of the n^- drift region. For blocking voltage of 2000 V, 25 µm thick drift region with a doping concentration of $3x10^{15}$ cm^{-3} was chosen.

Figure 2 shows 2D device simulation for 4H-SiC DiMOSFETs with JFET gaps ranging from 2 µm to 5 µm using Microtec software. An effective channel mobility of 50 cm^2/Vs, a gate oxide thickness of 500 Å, a gate length of 2 µm, and V_{GS}-V_{TH} of 10 V were used for on-state simulations. It is shown that the peak field in the gate oxide decreases for smaller JFET gaps. It is also shown that if the JFET gap is too small, specific on-resistance increases significantly. It is determined that the optimal JFET gap is 3 µm. However, JFET gap of 5 µm was used to account for implant straggles and other process biases.

The p-wells were formed by Aluminum implantation, with a total dose of $2x10^{13}$ cm^{-2}. Then, heavy Aluminum implantation was done to form p^+ contacts at the center of the p-wells, followed by a Nitrogen implantation to form n^+ source regions. All implantations were done using 1.6 µm thick densified PECVD oxide layers as implant masks. All the implants were activated at around 1600 ^oC in Ar under silicon overpressure. A 2 µm thick oxide layer was then deposited and patterned as thick field oxide followed by a gate oxidation. The gate oxides are either thermally grown or deposited by LPCVD (~500 Å) and annealed in an oxidizing ambient. Then, a 0.5 µm thick Moly layer was sputtered and patterned as gate metal. The contacts to source, drain and p^+ regions are formed with 0.1 µm thick Ni. A 1.5 µm thick PECVD oxide layer was then deposited using PECVD as an inter-metallic dielectric, and via holes were opened. Finally, a 2 µm thick Ti/Pt/Au layer is lifted-off as the final metal layer.

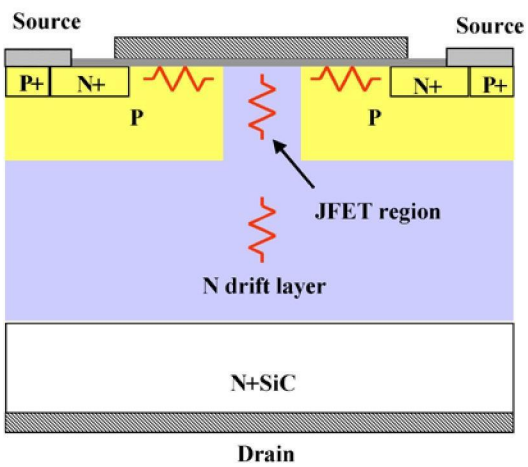


Fig. 1: A simple cross-sectional view of a 4H-SiC DiMOSFET.

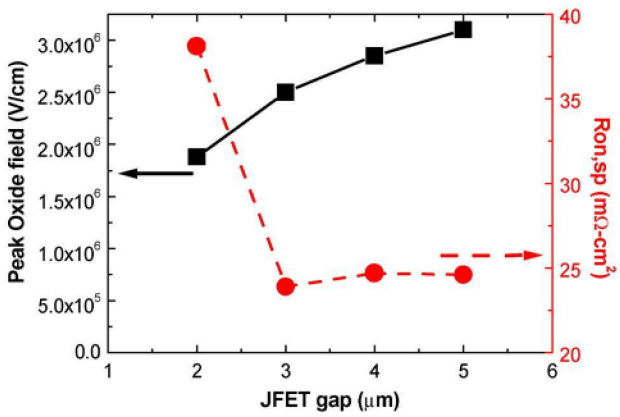


Fig. 2: 2D-device simulation results for different JFET gaps.

EXPERIMENTAL RESULTS

DiMOSFETs with NO anneal

The greatest challenge for 4H-SiC MOS devices is extremely low effective MOS channel mobility. Recently, anneal of gate oxide layer using nitric oxide (NO) was shown to be very effective in moving surface states near conduction band to lower half of the bandgap in 4H-SiC [4], which resulted in higher effective channel mobility on lightly doped p-type epilayers [5]. Figure 3 shows effective channel mobility (μ_{eff}) measured from FATFETs in implanted p-wells. 500Å thick deposited oxide layers were used as gate dielectric material. V_{DS} was fixed at 50 mV, and W/L was 100 µm/100 µm. It was shown that the MOSFETs with NO anneal,which was performed at Auburn University, have significantly higher μ_{eff} than the devices that did not receive NO anneals. However, measured peak μ_{eff} value was significantly lower than that reported in [5]. Figure 4 shows I-V characteristics of a power DiMOSFET fabricated using the NO anneal. This device had an active area of 0.00453 cm^2 (0.75 mm x 0.75 mm) and a cell pitch of 25 µm. A specific on-resistance value of 55 mΩ-cm^2 was measured at a V_{GS} of 25 V as shown in Fig 4 (a). However, at this gate bias the E-field in the gate oxide reaches 5 MV/cm. This stresses the gate oxide, and is not desirable for reliable power MOSFET operations. Greater value of μ_{eff} is needed to reduce E-field in the gate oxide in the on-state, and further optimization is necessary in MOS surface passivation in implanted p-wells.

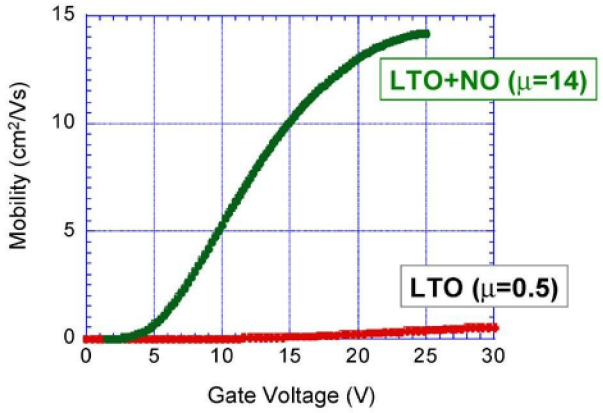
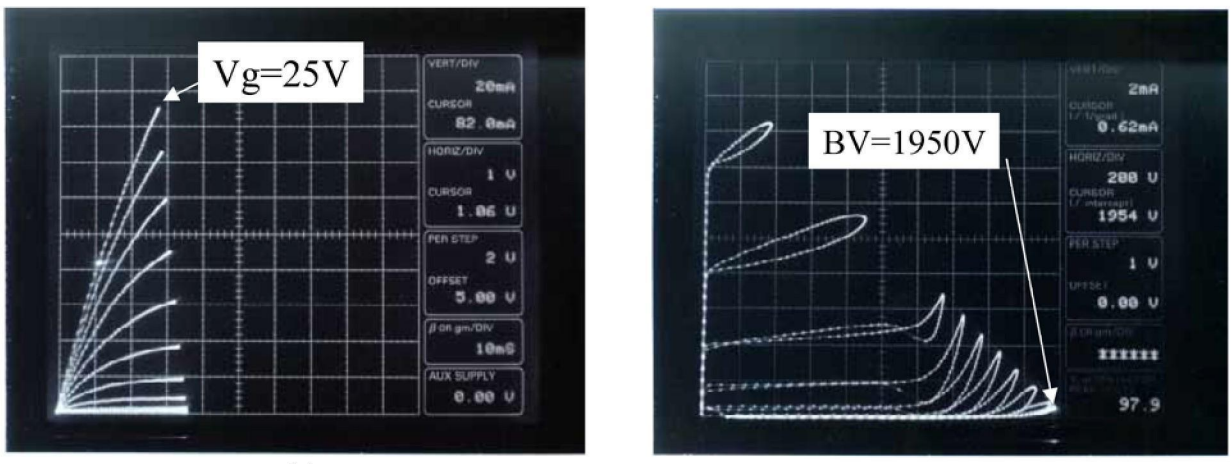


Fig. 3: Effective channel mobility extracted from 100µm/100µm FATFETs on implanted p-wells. NO anneal was done at Auburn University. (Courtesy of Prof. J. R. Williams)



(a) **(b)**

Fig. 4: IV characteristics of a DiMOSFET. The gate oxide was NO annealed at Auburn University [4], the cell pitch was 25 µm, and the active area was 0.00453cm^2.

Figure 4 (b) shows the blocking characteristics of this device. The device was capable of blocking 1950V. It was also observed that the breakdown voltage decreases as positive gate biases were applied. This suggests that open-base bipolar breakdown is happening at the edges of the p-wells due to high resistance in the implanted p-well regions, which had only $2x10^{13}$ cm^{-2} total implant dose. Increase in p-well implant dose is expected to alleviate this problem.

Buried Channel Structure

Another method for increasing μ_{eff} is forming a thin, lightly doped n-type buried layer in the MOS channel regions [2]. A BC (Buried-Channel) structure with a total n-type charge of $2.7x10^{12}$ cm^{-2} was formed into the channel region as shown in Fig. 5. A 500Å thick thermal oxide with a 950 °C re-Ox anneal [6] was used as gate dielectric. FATFET (W/L=100 µm/100 µm) measurements showed that these devices are normally on (Fig. 6), with a V_{TH} of –2 V. A peak μ_{eff} value of 194 cm^2/Vs was measured at V_{GS} = 2 V when the p-well grounded. At low values of V_{GS}, effects of bulk channel in the buried n-channel layer was measured, resulting in high μ_{eff}, while at high values of V_{GS}, significantly lower surface channel mobility was measured (μ_{eff} = ~25 cm^2/Vs at V_{GS} = 20 V).

Figure 6 shows the effect of p-well bias on μ_{eff}. When negative bias was applied to the p-well, peak μ_{eff} value decreased with the bias. At the same time, V_{TH} shifted positive, making this device normally off for p-well biases of –4V or greater. Application of negative bias to the p-well expands the depletion region of the buried pn junction, and reduces bulk channel in the buried n-channel layer. Similar results can be achieved if charge in the BC channel layer is reduced accordingly. It is expected that a BC structure with a charge of $1x10^{12}cm^{-2}$ in the buried n-layer can produce a normally off device with an effective mobility corresponding to the curve labeled $V_{p\text{-well}}$ = -4 V (dashed line) in Fig. 6.

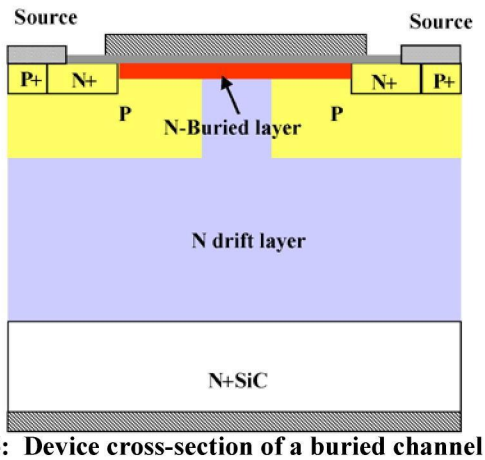


Fig. 5: Device cross-section of a buried channel device.

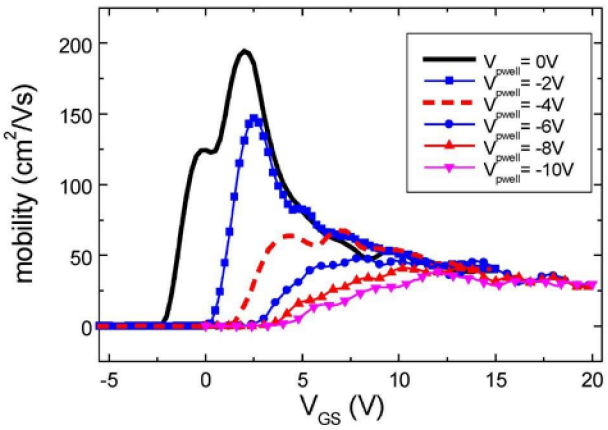
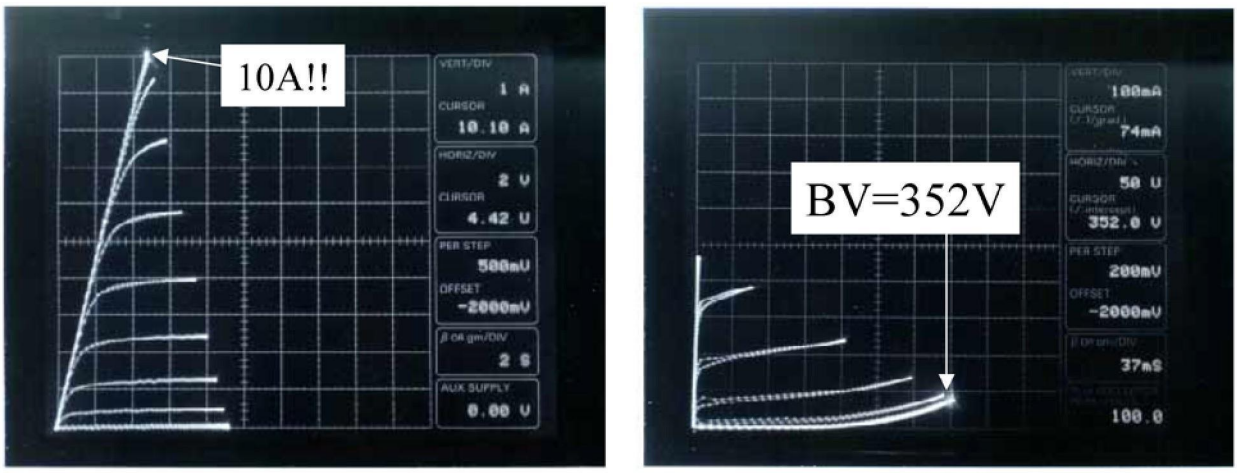


Fig. 6: Effective channel mobility extracted from 100µm/100µm FATFET with buried channel structure. Buried channel charge was $2.7x10^{12}cm^{-2}$.

Fig. 7 shows (a) the forward and (b) blocking I-V curves on the large power device (3.3 mm x 3.3 mm) with a BC layer with a sheet charge of $2.7x10^{12}cm^{-2}$. The device was slightly on and could be pinched off with -2 V on the gate. It showed a drain current of 10 A, which is the highest current reported in SiC power MOSFETs to date, at a forward drop of 4.4 V with a gate bias of only 2.5 V. A specific on-resistance ($R_{on,sp}$) value of about 43 mΩ-cm^2, was measured. It should be noticed that the increase in V_{GS} determined the saturation drain current, but had very

little effect on $R_{on,sp}$. This is due to the higher effective channel mobility, and MOSFET channel resistance no longer being the most dominant factor in determining $R_{on,sp}$ of this device. Blocking characteristics are shown in Fig. 7 (b). Blocking voltage of this device was limited by the leakage current, which was 74 mA at V_{DS} = 350 V and V_{GS} = -2 V. This leakage current was possibly caused by material defects, such as screw dislocations.



(a) (b)

Fig. 7: IV characteristics of a DiMOSFET with a buried channel layer. The charge in the buried n-layer was $2.7x10^{12}cm^{-2}$, the cell pitch was 25 μm, and the active area was $0.105cm^2$.

Figure 8 shows the specific on resistances ($R_{on,sp}$) of 0.75 mm x 0.75 mm devices with different pitches. It is shown that the specific on-resistance can be reduced by using a tighter cell pitch. A device with a pitch of 25 μm showed a $R_{on,sp}$ value of 37 mΩ-cm^2 while a device with a cell pitch of 16 μm showed a $R_{on,sp}$ value of 23 mΩ-cm^2 (Fig. 9). This clearly suggests that the JFET resistance is dominant in these devices. The specific on-resistance can be minimized by reducing the cell pitch, which increases JFET gate periphery per unit area.

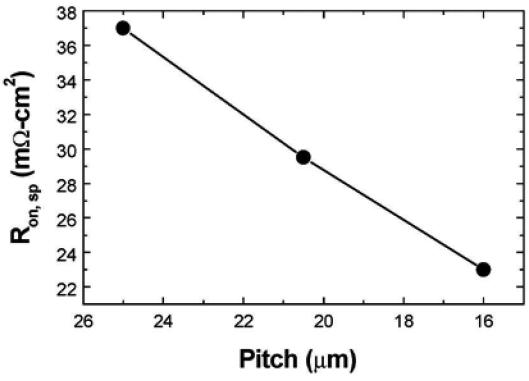


Fig. 8: Specific on-resistance decreases with cell pitch.

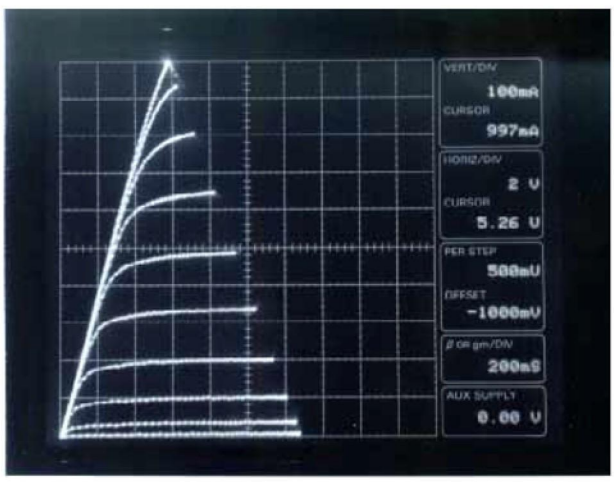


Fig.9: I-V characteristics of a 0.75 mm x 0.75 mm DiMOSFET (active area = $0.00453cm^2$) with a cell pitch of 16 μm. A $R_{on,sp}$ value of 23 mΩ-cm^2 was measured.

SUMMARY

In SiC DiMOSFETs, optimal JFET gap must be found so that adequate gate oxide protection is provided without increasing on-resistance excessively. 2D device simulations showed that 3 μm JFET gap was optimal for 2000 V 4H-SiC DiMOSFET with 25 μm thick, $3x10^{15}cm^{-3}$ doped drift layer. The other issue is extremely low effective channel mobility for 4H-SiC MOS devices in implanted p-wells. NO anneal, which was shown to be very promising for SiC MOSFETS in p-type epilayers, did not produce reasonable μ_{eff} for 4H-MOS devices in the implanted p-well. Buried channel (BC) structure with a channel charge of $2.7x10^{12}$ cm^{-2} showed high μ_{eff} ($194cm^2/Vs$ at V_{GS} = 2 V), but resulted in a normally on device (V_{TH} = -2 V). However, it was also shown that by controlling the charge in the of buried channel layer, a normally off device with high μ_{eff} can be produced. A 3.3 mm x 3.3 mm DiMOSFET with buried channel design showed a drain current of 10 A, which is the highest current reported in SiC power MOSFETs to date, at a forward drop of 4.4 V with a gate bias of only 2.5 V. For buried channel DiMOSFETs, specific on resistance was dominated by JFET resistance instead of MOSFET channel resistance. JFET resistance can be minimized by decreasing the device cell pitch. A specific on resistance value of 23 $m\Omega\text{-}cm^2$ was measured from a 0.75μm x 0.75 μm device with a cell pitch of 16 μm.

ACKNOWLEDGMENTS

This work is supported by DARPA and ONR under contract #N00014-99-C-0377, monitored by Dr. D. Radack and Dr. G. Campisi. Authors would also like to thank Prof. J. R. Williams at Auburn University for NO anneals.

REFERENCES

[1] J. N. Shenoy, J. A. Cooper, Jr., and M. R. Melloch, "High-Voltage Double-Implanted Power MOSFETs in 6H-SiC," *IEEE Electron Device Letters,* Vol. 18, pp. 93 - 95, March 1997.
[2] K. Ueno and T. Oikawa, "Counter-Doped MOSFET's of 4H-SiC," *IEEE Electron Device Letters*, Vol. 20, No. 12, pp. 624 – 626, December 1999.
[3] S. Dimitrijev, H.-F. Li, H. B. Harrison, and D. Sweatman, "Nitridation of Silicon dioxide Films Grown on 6H Silicon Carbide," *IEEE Electron Device Letters*, vol. 18, pp. 175-177, May 1997.
[4] G. Y. Chung, C. C. Tin, J. R. Williams, J. K. McDonald, M. Di Ventra, S. T. Pantelides, L. C. Feldman, R. A. Weller, "Effect of nitric oxide annealing on the interface trap densities near the band edges in the 4H polytype of silicon carbide," *Applied Physics Letters*, 76(13) pp. 1713-1715, March 2000.
[5] M. K. Das, L. A. Lipkin, J. W. Palmour, G. Y. Chung, J. R. Williams, K. McDonald, and L.C. Feldman, "High Mobility 4H-SiC Inversion Mode MOSFETs Using Thermally Grown, NO Annealed SiO_2," *presented at 58th IEEE Device Research Conference*, Denver, CO. June 19-21, 2000.
[6] L. A. Lipkin, D. B. Slater Jr, J. W. Palmour, "Low interface state density oxides on p-type SiC," *Trans Tech Publications. Materials Science Forum, vol.264-268, pt.2,* 1998, pp.853-6. Switzerland.